CLAIMS

What is claimed is:

1. A method of modeling a light emitting diode device comprising:

automatically generating a netlist from a computer-aided design layout; and

executing the netlist to produce an output correlative to current spreading uniformity for the light emitting diode device.

2. The method, as set forth in claim 1, wherein automatically generating a netlist comprises automatically generating a netlist having at least 60,000 lines.

3. The method, as set forth in claim 1, comprising producing a plurality of contour plots correlative to the current spreading uniformity for the light emitting diode device.

4. The method, as set forth in claim 1, comprising producing an output correlative to thermal performance of the light emitting diode device.

5. The method, as set forth in claim 1, comprising producing an output correlative to optical performance of the light emitting diode device.

6. A method of modeling a light emitting diode device comprising:

generating a computer-aided design layout of the light emitting diode device;

fracturing the layout to convert design geometries into orthogonal rectangles defined by coordinates;

scaling the layout to a specified element size, wherein the scaled layout includes each of a plurality of nodes, a plurality of resistors and a

plurality of diodes each having a layer number and a unique coordinate associated therewith;

automatically generating a netlist from the scaled layout; and

executing the netlist to produce an output correlative to current spreading uniformity for the light emitting diode device.

7. The method, as set forth in claim 6, comprising producing a plurality of contour plots correlative to the current spreading uniformity for the light emitting diode device.

8. The method, as set forth in claim 6, comprising producing a tabular output correlative to the current spreading uniformity for the light emitting diode device.

9. The method, as set forth in claim 6, comprising naming each of the nodes such that a name of each node includes the layer number and the unique coordinate associated therewith.

10. The method, as set forth in claim 6, comprising naming each of the elements such that a name of each element includes an element type, the layer number and the unique coordinate associated therewith.

11. The method, as set forth in claim 6, comprising before executing the netlist, manually supplementing the netlist with information correlative two power connections.

12. The method, as set forth in claim 6, comprising before executing the netlist, manually supplementing the netlist with information correlative to elements oriented in the vertical direction of the light emitting diode device.

13. The method, as set forth in claim 6, comprising before generating the netlist, automatically eliminating any of the plurality of nodes having less than two of the plurality of resistors coupled thereto.

14. A method of modeling a light emitting diode device comprising:

fracturing a computer aided design layout corresponding to the light emitting diode device to convert design geometries into orthogonal rectangles defined by coordinates;

scaling the layout to a specified element size;

adding a corresponding layer number and element value to elements and nodes in each of the orthogonal rectangles;

automatically generating a netlist from the scaled layout;

executing the netlist to produce a simulation output file;

calculating currents associated with each of the elements; and

producing a current output file comprising the currents associated with each of the elements.

15. The method, as set forth in claim 14, comprising converting the simulation output file into tabular form.

16. The method, as set forth in claim 14, comprising producing a plurality of contour plots from the current output file, wherein the contour plots are correlative to the current spreading uniformity of the light emitting diode device.

17. The method, as set forth in claim 14, comprising naming each of the elements such that a name of each element includes an element type, the layer number and the unique coordinate associated therewith.

18. The method, as set forth in claim 14, comprising naming each of the nodes such that a name of each node includes the layer number and the unique coordinate associated therewith.

19. The method, as set forth in claim 14, comprising before generating the netlist, automatically eliminating any of the nodes having less than two of the elements coupled thereto.

20. A method of modeling a light emitting diode device comprising:

automatically generating a netlist from a computer-aided design layout of the light emitting diode device, wherein the design layout comprises each of a plurality of nodes, a plurality of resistors and a plurality of diodes;

uniquely naming each of the plurality of nodes, the plurality of resistors and the plurality of diodes in accordance with location within the design layout to produce a unique name corresponding therewith; and

modeling the light emitting diode device using the netlist to produce a modeling output, wherein the modeling output comprises the unique name corresponding to each of the plurality of nodes, the plurality of resistors and the plurality of diodes.

21. The method, as set forth in claim 20, wherein uniquely naming each of the plurality of resistors and each of the diodes comprises producing a unique name corresponding therewith and comprising an element type, a layer number and a unique coordinate associated therewith.

22. The method, as set forth in claim 20, wherein uniquely naming each of the plurality of nodes comprises producing a unique name corresponding therewith and comprising a layer number and the unique coordinate associated therewith.

23. A computer-readable medium storing computer instructions for:

automatically generating a netlist from a computer-aided design layout corresponding to a light emitting diode device.

24. A computer-readable medium storing computer instructions for:

fracturing a computer-aided design layout corresponding to a light emitting diode device to convert design geometries into orthogonal rectangles defined by coordinates;

scaling the layout to a specified element size, wherein the scaled layout includes each of a plurality of nodes, a plurality of resistors and a plurality of diodes each having a layer number and a unique coordinate associated therewith; and

automatically generating a netlist from the scaled layout.

25. The computer-readable medium, as set forth in claim 24, comprising computer instructions for before generating the netlist, automatically eliminating any of the plurality of nodes having less than two of the plurality of resistors coupled thereto.

26. The computer-readable medium, as set forth in claim 24, comprising computer instructions for producing a plurality of contour plots correlative to the current spreading uniformity for the light emitting diode device.

27. The computer-readable medium, as set forth in claim 24, comprising computer instructions for producing a tabular output correlative to the current spreading uniformity for the light emitting diode device.

28. A computer-readable medium storing computer instructions for:

fracturing a computer aided design layout corresponding to a light emitting diode device to convert design geometries into orthogonal rectangles defined by coordinates;

scaling the layout to a specified element size;

adding a corresponding layer number and element value to elements and nodes in each of the orthogonal rectangles;

automatically generating a netlist from the scaled layout; and

producing a contour plot corresponding to current uniformity in the light emitting diode device and correlative to an executed simulation of the netlist.